

10/709,113

1. (Currently Amended) A bipolar device comprising:
  - a base;
  - an emitter above said base, wherein said emitter has a T-shape with a lower section and an upper section that is wider than said lower section;
  - spacers adjacent said lower section of said emitter and beneath said upper section of said emitter; and
  - non-silicided material adjacent said spacers; and
  - a silicide layer adjacent said ~~spacers~~ non-silicided material and beneath said upper section of said emitter, wherein said non-silicided material is positioned between said spacers and said silicide layer.
2. (Currently Amended) ~~The device in claim 1 further comprising,~~ A bipolar device comprising:
  - a base;
  - an emitter above said base, wherein said emitter has a T-shape with a lower section and an upper section that is wider than said lower section;
  - spacers adjacent said lower section of said emitter and beneath said upper section of said emitter;
  - a silicide layer adjacent said spacers and beneath said upper section of said emitter; and
  - a dielectric structure over said base and beneath said spacers.
3. (Original) The device in claim 2, wherein said base is wider than said dielectric structure.
4. (Original) The device in claim 1, wherein said spacers separate said emitter from said silicide.
5. (Original) The device in claim 1, wherein said base comprises:

10/709,113

an intrinsic base; and

an extrinsic base above said intrinsic base.

6. (Original) The device in claim 1, wherein said spacers comprise insulators.

7. (Original) The device in claim 1, wherein said silicide comprises a salicide.

8. (Currently Amended) A transistor device comprising:

a lower semiconductor structure having a first-type impurity;

a middle semiconductor region above said lower semiconductor structure, said middle semiconductor region having a second-type impurity complementary to said first-type impurity;

an upper semiconductor structure above said middle semiconductor region, wherein said emitter has a T-shape with a lower section and an upper section that is wider than said lower section;

spacers adjacent said lower section of said emitter and beneath said upper section of said emitter; and

non-silicided material adjacent said spacers; and

a silicide layer adjacent said ~~spacers~~ non-silicided material and beneath said upper section of said emitter, wherein said non-silicided material is positioned between said spacers and said silicide layer.

9. (Currently Amended) ~~The device in claim 8 further comprising,~~ A transistor device comprising:

a lower semiconductor structure having a first-type impurity;

a middle semiconductor region above said lower semiconductor structure, said middle semiconductor region having a second-type impurity complementary to said first-type impurity;

an upper semiconductor structure above said middle semiconductor region, wherein said emitter has a T-shape with a lower section and an upper section that is wider than said lower section;

10/709,113

spacers adjacent said lower section of said emitter and beneath said upper section of said emitter;

a silicide layer adjacent said spacers and beneath said upper section of said emitter, and  
a dielectric structure over said middle semiconductor region and beneath said spacers.

10. (Original) The device in claim 9, wherein said middle semiconductor region is wider than said dielectric structure.

11. (Original) The device in claim 8, wherein said spacers separate said emitter from said silicide.

12. (Original) The device in claim 8, wherein said middle semiconductor region comprises:  
an intrinsic middle semiconductor region; and  
an extrinsic middle semiconductor region above said intrinsic middle semiconductor region.

13. (Original) The device in claim 8, wherein said spacers comprise insulators.

14. (Original) The device in claim 8, wherein said silicide comprises a silicide.

15-31 (Cancelled).